

WHAT IS CLAIMED IS:

- 5 1. A phase detector comprising:
 a first flip flop comprising:
 a data input coupled to a first signal having a
 first frequency, and
 a clock input coupled to a second signal having a
10 second frequency, wherein the first frequency is a
 multiple of the second frequency; and
 a second flip flop comprising:
 a data input coupled to an output of the first flip
 flop, and
15 a clock input coupled to the second signal.
2. The phase detector of claim 1 wherein the first flip
flop comprises a high speed flip flop.
- 20 3. The phase detector of claim 2 wherein the high speed
flip flop comprises at least one inductive load.
4. The phase detector of claim 2 wherein the second
flip flop comprises a low speed flip flop.
- 25 5. The phase detector of claim 1 wherein the first flip
flop comprises a high speed latch and a low speed latch.
6. The phase detector of claim 5 wherein the high speed
30 latch comprises at least one inductive load.
7. The phase detector of claim 1 wherein:
 the data input of the first flip flop comprises a first
differential input;

the data input of the second flip flop comprises a second
5 differential input; and

the clock inputs of the first and second flip flops
comprise differential clock inputs.

8. A phase detector comprising:
10 a high speed flip flop having a data input coupled to a
first clock signal at a first clock frequency and a clock
input coupled to a second clock signal at a second clock
frequency wherein the first clock frequency is a multiple of
the second clock frequency and wherein the high speed flip
15 flop comprises a high speed latch and a low speed latch.

9. The phase detector of claim 8 wherein the high speed
flip flop comprises at least one inductive load.

20 10. A method of detecting relative phase of a plurality
of signals, the method comprising:

providing a first signal, having a first frequency, to a
data input of a first flip flop;

clocking the first flip flop using a second signal,
25 having a second frequency, wherein the first frequency is a
multiple of the second frequency;

providing an output of the first flip flop to a second
flip flop;

clocking the second flip flop using the second signal;
30 and

generating at least one output signal of the second flip
flop indicative of a phase difference between the first signal
and the second signal.

5 11. The method of claim 10 wherein the at least one output signal is indicative of a whether the second signal leads the first signal or whether the second signal lags the first signal.

10 12. The method of claim 10 comprising delaying the second signal according to the at least one output signal.

15 13. The method of claim 10 wherein:
the first signal comprises a first differential signal;
the second signal comprises a second differential signal;
and
the output signal comprises a differential output signal.

20 14. The method of claim 10 comprising driving an inductive load for the first flip flop.

25 15. A delay lock loop comprising:
phase detector comprising:
a first flip flop comprising a data input coupled to a first signal having a first frequency, a clock input coupled to a second signal having a second frequency, wherein the first frequency is a multiple of the second frequency, and at least one output; and
a second flip flop comprising a data input coupled to the at least one output of the first flip flop, a clock input coupled to the second signal, and at least one output for generating at least one phase error signal;
a digital filter, coupled to receive the at least one phase error signal, that generates at least one filtered
35 signal; and

5 a phase rotator, coupled to receive the at least one
filtered signal and the second signal, that delays the second
signal according to the at least one filtered signal.

10 16. The delay lock loop of claim 15 wherein the first
flip flop comprises a high speed latch and a low speed latch.

17. The delay lock loop of claim 16 wherein the high
speed latch comprises at least one inductive load.

15 18. The delay lock loop of claim 15 wherein:
the data input of the first flip flop comprises a first
differential input;

the data input of the second flip flop comprises a second
differential input; and

20 the clock inputs of the first and second flip flops
comprise differential clock inputs.

19. A phase lock loop comprising:
phase detector comprising:

25 a first flip flop comprising a data input coupled to
a first signal having a first frequency, a clock input
coupled to a second signal having a second frequency,
wherein the first frequency is a multiple of the second
frequency, and at least one output; and

30 a second flip flop comprising a data input coupled
to the at least one output of the first flip flop, a
clock input coupled to the second signal, and at least
one output for generating at least one phase error
signal;

35 a charge pump, coupled to receive the at least one phase
error signal, that generates at least one current signal;

5 a loop filter, coupled to receive the at least one
current signal, that generates at least one filtered signal;
and

10 a delay circuit, coupled to receive the at least one
filtered signal and the second signal, that delays the second
signal according to the at least one filtered signal.

20. The phase lock loop of claim 19 wherein the delay
circuit comprises at least one delay line.

15 21. The phase lock loop of claim 19 wherein the first
flip flop comprises a high speed latch and a low speed latch.

22. The phase lock loop of claim 21 wherein the high
speed latch comprises at least one inductive load.

20 23. The phase lock loop of claim 19 wherein:
the data input of the first flip flop comprises a first
differential input;
the data input of the second flip flop comprises a second
differential input; and
25 the clock inputs of the first and second flip flops
comprise differential clock inputs.

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